AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend Claims 17 and 21 as follows:

1-16. (Canceled)

17. (Currently Amended) A method of making a heterojunction bipolar transistor, comprising the steps of:

providing an emitter/base layer having a generally flat base-surface;

providing that said emitter/base layer includes an emitter portion selected from one or more of the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon, and a base portion selected from one or more of the group Si, Ge and SiGe;

providing that said base portion includes a generally flat base surface;

processing said base-surface to produce a base-surface that is compatible with direct-wafer-bonding;

providing a collector layer;

providing that said collector layer is selected from one or more of the group SiC, (4H, 6H, 15R, 3C .....);

providing that said collector layer includes a generally-flat collector-surface;

processing said collector-surface to produce a collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said base-surface to said collector-surface.

18. (Original) The method of claim 17 including the steps of:

providing that said collector layer includes a second-surface that extends generally parallel to said collector-surface;

processing said second-surface to produce a second-surface that is compatible with direct-wafer-bonding;

providing a sub-collector layer having a generally flat sub-collector-surface;

processing said sub-collector-surface to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

19. (Original) The method of claim 17 including the steps of:

providing that said emitter/base layer includes the number of emitter-portions, each having an emitter-surface that is compatible with direct-wafer-bonding;

providing a number of physically spaced base-portions, each having a base-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding each individual one of said emitter surfaces to an individual one of said base-surfaces.

20. (Original) The method of claim 19 including the steps of:

providing that said collector layer includes a second-surface that extends generally parallel to said collector-surface;

processing said second-surface to produce a second-surface that is compatible with direct-wafer-bonding;

providing a sub-collector layer having a generally flat sub-collector-surface;

processing said sub-collector-surface to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

21. (Currently Amended) The method of claim [[14]]17 including the steps of:

providing that said emitter/base layer includes an emitter-portion and a base-portion; and

providing that a bandgap of said emitter-portion and a bandgap of said collector layer are larger than a bandgap of said base-portion.

22. (Original) The method of claim 21 including the steps of:

providing that said collector layer includes a second-surface that extends generally parallel to said collector-surface;

processing said second-surface to produce a second-surface that is compatible with direct-wafer-bonding;

providing a sub-collector layer having a generally flat sub-collector-surface;

processing said sub-collector-surface to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

23-29. (Canceled)

30. (Previously Presented) A method of making a heterojunction bipolar transistor, comprising the steps:

processing a collector-surface of a collector layer and a base-surface of an emitter/base structure to produce a collector-surface and base-surface, respectively, that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said base-surface to said collector-surface, wherein said emitter/base structure includes an emitter portion selected from one or more of the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon and a base portion

selected from one or more of the group Si, Ge and SiGe and wherein said collector layer comprises SiC.

31. (Previously Presented) The method of claim 30 further comprising:

processing a second-surface of the collector to produce a second-surface that is compatible with direct-wafer-bonding;

processing a sub-collector-surface of a sub-collector layer to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said second-surface to said sub-collector-surface.

32. (Previously Presented) The method of claim 30 wherein said emitter/base structure includes a number of emitter-portions, each having an emitter-surface that is compatible with direct-wafer-bonding, and a number of physically spaced base-portions, each having a base-surface that is compatible with direct-wafer-bonding and further comprising:

direct-wafer-bonding each individual one of said emitter surfaces to an individual one of said base-surfaces.

33. (Previously Presented) The method of claim 30 wherein said base portion is Si.

34. (Previously Presented) The method of claim 30 wherein said base portion comprises Ge.

35. (Previously Presented) The method of claim 30, wherein said emitter portion is Si.

36. (Previously Presented) The method of claim 30, wherein said emitter portion comprises Ge.

37. (Previously Presented) The method of claim 30, wherein said emitter portion comprises amorphous-Si.

38. (Previously Presented) The method of claim 30, wherein said emitter portion comprises amorphous-SiC.

39. (Previously Presented) The method of claim 30, wherein said emitter portion comprises diamond-like carbon.

40. (Previously Presented) The method of claim 30 wherein a bandgap of said emitter portion and a bandgap of said collector layer are larger than a bandgap of said base portion.

41. (Previously Presented) A method of making a heterojunction bipolar transistor, comprising the steps:

processing a base-surface of a base layer and an emitter-surface of an emitter structure to produce a base-surface and an emitter-surface, respectively, that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said emitter-surface to said base-surface, wherein said emitter structure comprises a material that is selected from one or more of the group Si, SiGe, SiC, amorphous-Si, amorphous-SiC and diamond-like carbon, the base layer is selected from one or more of the group Si, Ge and SiGe and wherein said transistor comprises a collector layer, the collector layer comprising SiC.

42. (Previously Presented) The method of claim 41 further comprising:

processing a first-surface of the collector layer to produce a first-surface that is compatible with direct-wafer-bonding;

processing a second-surface of the base layer to produce a second-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said first-surface to said second-surface.

43. (Previously Presented) The method of claim 41 further comprising::

processing a first-surface of the collector layer to produce a first-surface that is compatible with direct-wafer-bonding;

processing a sub-collector-surface of a sub-collector layer to produce a sub-collector-surface that is compatible with direct-wafer-bonding; and

direct-wafer-bonding said first-surface to said sub-collector-surface.

44. (Previously Presented) The method of claim 41 wherein said emitter structure includes a number of emitter-portions, each having an emitter-surface that is compatible with direct-wafer-bonding, and a number of physically spaced base-portions, each having a base-surface that is compatible with direct-wafer-bonding and further comprising:

direct-wafer-bonding each individual one of said emitter surfaces to an individual one of said base-surfaces.

45. (Previously Presented) The method of claim 41 wherein said base layer is Si.

46. (Previously Presented) The method of claim 41 wherein said base layer comprises Ge.

47. (Previously Presented) The method of claim 41, wherein said emitter material is Si.

48. (Previously Presented) The method of claim 41, wherein said emitter material comprises Ge.

49. (Previously Presented) The method of claim 41, wherein said emitter material comprises amorphous-Si.

50. (Previously Presented) The method of claim 41, wherein said emitter material comprises amorphous-SiC.

51. (Previously Presented) The method of claim 41, wherein said emitter material comprises diamond-like carbon.

52. (Previously Presented) The method of claim 41 wherein a bandgap of said emitter structure and a bandgap of said collector layer are larger than a bandgap of said base layer.